The Libre-SOC Gigabit Router ASIC

An entirely Libre-Licensed ASIC
with Gigabit Ethernet ports and USB2
and full Libre Firmware

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Why a Libre Gigabit Router?

- Most Router ASICs are proprietary
- Persistent GPL violations
- Could contain unknown spying back-doors
  nobody can tell
- Full HDL and Firmware means it's fully-auditable

Who?

- Luke Leighton (Libre-SOC)
  Lead developer

- Jean-Paul Chaput,
  Dmitry Galayko,
  Marie-Minerve Louerat
  LIP6.fr, Sorbonne University
  Developers of Coriolis2 VLSI

- Staf Verhaegen
  Chips4Makers.io Belgium
  Developer of FlexLib Cell Libraries

What?

- Vector Processor based on the Power ISA, (Draft) SVP64 Cray Vectors and efficient packet processing instructions
- Gigabit Ethernet Ports (RGMII) USB2 ports (USB-ULPI), GPIO, I2C, QSPI etc.
- DMA Engine to handle fast transfer between Ethernet Ports
- Analog PLL (Libre-Licensed, no NDA)
- Lots of simulations and FPGA testing
- Put it all together: MPW Shuttle Runs
  to be tested, report published
- All entirely Libre-Licensed
  as best we can comply with Foundry NDAs

How?

- Entirely in nmigen HDL (python-based, Libre-Licensed)
- Huge ancillary spin-off libraries created:
- IEEE754 pipelined FPU, SIMD Library, I/O HDL Library
- Power ISA now in Machine-readable form
- Coriolis2 VLSI now silicon-proven in 10x larger automated layouts (800,000 gates)
- No NDAs, no commercial confidential agreements signed means full Academic and Ethical Freedom to talk about what we did and how we did it

The end

Thank you

Questions?

- Discussion: http://lists.libre-soc.org
- Libera IRC #libre-soc
- http://libre-soc.org/
- http://coriolis.lip6.fr
- http://chips4makers.io