RFC02601 (r2): Byte-Reverse Instructions

Severity: Major

Status: New

Date: July 5, 2018

Target Version: 3.1

Source Version: 3.0B

Books and sections affected:

Book I: Section 3.3.17 Byte-Reverse Instructions (new section)

Appendices: Appendix D. Power ISA Instruction Set Sorted by Opcode
Appendix E. Power ISA Instruction Set Sorted by Version
Appendix F. Power ISA Instruction Set Sorted by Mnemonic

Summary: New instructions
Byte-Reverse Halfword X-form
Byte-Reverse Word X-form
Byte-Reverse Doubleword X-form

Submitter: Brett Olsson, IBM

Requester: Anton Blanchard, IBM

Impact on processor:
Addition of three new GPR-based byte-reverse instructions.

Impact on software:
Requires support for new instructions in assemblers, debuggers and related tools.

Keywords: byte-reverse, Little-Endian, radix MMU page table manipulation

Change History

Changes made June 5, 2018 (r2):

-
-
-

Changes made June 1, 2018 (r1):

- Fixed extended opcode for ***brh*** in instruction index.

Changes made April 20, 2017 (r0):

- Created RFC.

Motivation

Three new instructions that perform byte-reverse operations to alleviate issues with managing the Big-Endian-defined radix MMU in a Little-Endian environment.

Changes to the Books

Book I:

Section 3.3.17 Byte-Reverse Instructions (new section)

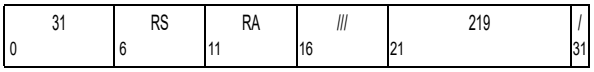
Add the following new Section and instruction descriptions.

---------- Begin text ----------

1.0.1 Byte-Reverse Instructions

Byte-Reverse Halfword X-form

brh RA,RS




```
RA ← (RS)8:15   || (RS)0:7   ||
     (RS)24:31  || (RS)16:23 ||
     (RS)40:47  || (RS)32:39 ||
     (RS)56:63  || (RS)48:55
```

The contents of bits 0:15 of register RS are placed into bits 0:15 of register RA in byte-reversed order.

The contents of bits 16:31 of register RS are placed into bits 16:31 of register RA in byte-reversed order.

The contents of bits 32:47 of register RS are placed into bits 32:47 of register RA in byte-reversed order.

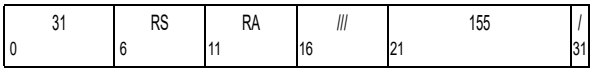
The contents of bits 48:63 of register RS are placed into bits 48:63 of register RA in byte-reversed order.

Special Registers Altered:

None

Byte-Reverse Word X-form

brw RA,RS




```
RA ← (RS)24:31 || (RS)16:23 ||
     (RS)8:15  || (RS)0:7   ||
     (RS)56:63 || (RS)48:55 ||
     (RS)40:47 || (RS)32:39
```

The contents of bits 0:31 of register RS are placed into bits 0:31 of register RA in byte-reversed order.

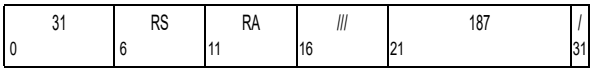
The contents of bits 32:63 of register RS are placed into bits 32:63 of register RA in byte-reversed order.

Special Registers Altered:

None

Byte-Reverse Doubleword X-form

brd RA,RS




```
RA ← (RS)56:63 || (RS)48:55 ||
     (RS)40:47 || (RS)32:39 ||
     (RS)24:31 || (RS)16:23 ||
     (RS)8:15  || (RS)0:7
```

The contents of register RS are placed into register RA in byte-reversed order.

Special Registers Altered:

None

---------- End text ----------

Appendices:

Appendix D. Power ISA Instruction Set Sorted by Opcode
Appendix E. Power ISA Instruction Set Sorted by Version
Appendix F. Power ISA Instruction Set Sorted by Mnemonic

Add the following entries to each table.

---------- Begin text ----------

011111 .... 00101 11011.	X	I	pg #	v3.0B			brd	Byte-Reverse Doubleword
011111 .... 00110 11011.	X	I	pg #	v3.0B			brh	Byte-Reverse Halfword
011111 .... 00100 11011.	X	I	pg #	v3.0B			brw	Byte-Reverse Word

---------- End text ----------

---------- End RFC ----------